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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,647	06/28/2001	Joo Soo Lim	8733.442.00	2011

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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,647	LIM, JOO SOO	
	Examiner	Art Unit	
	Prabodh M. Dharia	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-11 and 15* is/are allowed.

6)☒ Claim(s) *1-7 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. **Status:** Receipt is acknowledged of papers submitted on February 09, 2006 under amendments and reconsideration, which have been placed of record in the file. Claims 1-15 are pending in this action.

Response to Amendment

2. The amendments to claim 6 filed on 02-09-2006, is sufficient to overcome the objection to Claim 6. Therefore objection is withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8,10,12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita (6,275,061 B1) in view of Knodoh et al. (2003/0034944 A1) and Toyoda et al. (6,448,952 B1).

Regarding Claim 1, Tomita teaches a liquid crystal display panel (Col. 3, Lines 45-47, 48-59, Col. 4, Lines 45-64, Col.8, Lines 26-65, Col. 7, Lines 50-56, Col. 17, Lines 40-53, Col. 19, Lines 39-50, Col. 15, Lines 51-58, Col. 13, Lines 31,32), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53, 54) and a plurality of gate lines (Col.

3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and a plurality of liquid crystal pixel cells (Col. 8, Lines 12,13) arranged where the gate lines cross the data lines (Col. 4, Lines 45-64), the method comprising: applying data voltages to the data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53-55); applying a mode setting signal to a gate driver connected with the gate lines; sequentially scanning the gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel (Col. 8, Lines 48-65); and identifying any defective pixel cells among the plurality of liquid crystal pixel cells from the test pattern (Col. 7, Lines 50-56) and teaches a liquid crystal display device (Col. 3, Lines 45,46), comprising: a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53, 54) and a plurality of scanning lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and liquid crystal pixel cells arranged in a matrix (Col. 3, Lines 54,55, Col. 8, Lines 12,13); a data driver circuit for supplying data to the data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53-55); a scanning driver circuit for supplying scanning signals to the scanning lines (Col. 17, Lines 40-53, Col. 19, lines 39-50, Col. 15, Lines 51-58, Col. 13, Lines 31,32); and control means for controlling the data driver circuit and the scanning driver circuit (Col. 3, Lines 55-57, Col. 4, Lines 57-59), wherein said control means controls the scanning driver circuit (Col. 8, Lines 26-65).

However, Tomita fails to teach sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the liquid crystal display panel to display an image at an increased brightness.

However, Kondoh et al. teaches sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the liquid crystal display panel to display an image at an increased brightness (pages 5and 6, paragraph 47).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Kondoh et al. teaching in teaching of Tomita to be able to control scanning of a display in a reverse order and forward order to achieve uniform brightness.

Tomita teaches a method of testing a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and scanning the scanning lines in a sequence proceeding from low-order lines to high-order lines to display a test picture (Col. 8, Lines 48-65); and identifying any defective pixel cells among the plurality of liquid crystal pixel cells from the test pattern (Col. 7, Lines 50-56).

However, Tomita fails to teach reverse mode is set by a mode setting signal that is applied to a scanning driver circuit generating a scanning signal, to thereby indicate an application direction of the scanning signal and sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device.

However, Toyoda et al. teaches reverse mode is set by a mode setting signal (Col. 13, Lines 31-40. where L/R signal represents mode signal and generated using logic combinations of gates acting like a mode switch (col. 7, Lines 16-36 typical logic and gate generated signals (Col. 9, Line 1 to Col. 10, Line 19)) that is applied to a scanning driver circuit generating a scanning signal (Col. 13, Lines 31-40), to thereby indicate an application direction of the scanning signal

and sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device (Col.13, Lines 31-59).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Toyoda et al. teaching in teaching of Tomita to be able to improve stereoscopic image display device in which cross talk is suppressed without causing flicker.

Regarding Claim 2, Tomita teaches a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and a plurality of liquid crystal pixel cells (Col. 8, Lines 12,13) arranged where the gate lines cross the data lines (Col. 4, Lines 45-64).

Regarding Claim 3, Tomita teaches switching device consists of a thin film transistor (Col. 4, Lines 47,48) including a gate electrode connected to a corresponding one of the scanning lines to receive the scanning signal (Col. 3, Lines 55-57, Col. 4, Lines 57-59); a source electrode connected to a corresponding one of the data lines to receive said data (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54); and a drain electrode opposed to the source electrode with a desired channel there between and connected to a pixel electrode for driving the liquid crystal pixel cell (Col. 6, Lines 24-41, P-channel and N channel Col. 4, Lines 53-67).

Regarding Claim 4, Tomita teaches control means generates a gate start pulse for indicating a start position of the scanning signal, a mode setting signal for assigning an application direction of the scanning signal to any one of a forward direction and a reverse

direction, and an output enable signal for controlling an output of the scanning driver circuit (Col. 8, Lines 35-41, Col. 8, Lines 26-65, Col. 9, Line 62 to Col. 10, Line 3).

Regarding Claim 5, Tomita teaches control means applies a dot clock for indicating an application time of said data to the data driver circuit (Col. 8, Lines 35-41).

Regarding Claim 6, Tomita teaches scanning driver circuit consists of a bilateral shift register in which its shift direction is controlled in response to a mode setting signal (Col. 8, Lines 26-65, Col. 9, Line 62 to Col. 10, Line 3)

Regarding Claim 7, Tomita teaches control means controls the scanning driver circuit such that the liquid crystal display panel is scanned in a forward-sequential manner upon normal operation of the liquid crystal display panel (Col. 8, Lines 48-65).

Regarding Claim 12, Tomita teaches a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and a plurality of liquid crystal pixel cells (Col. 8, Lines 12,13) arranged where the gate lines cross the data lines (Col. 4, Lines 45-64), the method comprising: applying data voltages to the data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53-55); applying a mode setting signal to a gate driver connected with the gate lines; sequentially scanning the

gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel (Col. 8, Lines 48-65).

However, Tomita fails to teach a gate driver circuit for sequentially supplying a gate signal to the gate lines in a forward sequential order upon normal operation, and sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device to increase the brightness of the display upon testing compared to the brightness under normal operation.

However, Kondoh et al. teaches a gate driver circuit for sequentially supplying a gate signal (scan signal) to the gate lines in a forward sequential order upon normal operation, and sequentially supplying the gate signal (scan signal) to the gate lines in a reverse sequential order upon testing the device to increase the brightness of the display upon testing compared to the brightness under normal operation. (pages 5and 6, paragraph 47).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Kondoh et al. teaching in teaching of Tomita to be able to control scanning of a display in a reverse order and forward order to achieve uniform brightness.

Tomita teaches a method of testing a liquid crystal display panel (Col. 3, Lines 45-47), having a plurality of data lines (Col. 3, Lines 57-59, Col. 4, Lines 59,60, Col. 8, Lines 53, 54) and a plurality of gate lines (Col. 3, Lines 55-57, Col. 4, Lines 57-59) crossing each other (Col. 4, Lines 45-64) and scanning the scanning lines in a sequence proceeding from low-order lines to high-order lines to display a test picture (Col. 8, Lines 48-65); and identifying any defective pixel cells among the plurality of liquid crystal pixel cells from the test pattern (Col. 7, Lines 50-56).

However, Tomita fails to teach reverse mode is set by a mode setting signal that is applied to a scanning driver circuit generating a scanning signal, to thereby indicate an application direction of the scanning signal and sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device.

However, Toyoda et al. teaches reverse mode is set by a mode setting signal (Col. 13, Lines 31-40. where L/R signal represents mode signal and generated using logic combinations of gates acting like a mode switch (col. 7, Lines 16-36 typical logic and gate generated signals (Col. 9, Line 1 to Col. 10, Line 19)) that is applied to a scanning driver circuit generating a scanning signal (Col. 13, Lines 31-40), to thereby indicate an application direction of the scanning signal and sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device (Col.13, Lines 31-59).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Toyoda et al. teaching in teaching of Tomita to be able to improve stereoscopic image display device in which cross talk is suppressed without causing flicker.

Regarding Claim 13, Tomita teaches the gate driver circuit comprises a shift register having a control terminal for controlling a sequential order of supplying the gate signal to the gate lines (Col.8, Lines 48-65)

Regarding Claim 14, Tomita teaches a controller supplying a mode-setting signal to the control terminal (Col. 8, Lines 26-51).

Allowable Subject Matter

5. Claims 8-11 and 15 are allowed.

6. The following is an examiner's statement of reasons for allowance:

A method of testing a liquid crystal display panel, having a plurality of data lines and a plurality of gate lines crossing each other and a plurality of liquid crystal pixel cells arranged where the gate lines cross the data lines, the method comprising: applying data voltages to the data lines; **applying a mode setting signal to a gate driver connected with the gate lines; sequentially scanning the gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel at an increased brightness; and identifying any defective pixel cells among the plurality of liquid crystal pixel cells from the test pattern.**

The cited references on 892's fails to recite or disclose above bold underlined claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

7. Applicant's arguments with respect to claims 1,12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

10. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU269

March 19, 2006

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